1. (Amended) An integrated circuit for image frame rendering and DSP applications, the integrated circuit during operation operating with memory, the integrated circuit comprising:

an interface circuit configured to control access to said memory, the interface circuit coupled to said memory;

an embedded processor configured to control the integrated circuit, the embedded processor configured to control the interface circuit to receive information therefrom; and

an array processor for performing arithmetic calculations, the array processor coupled to the interface circuit to receive information therefrom and connected to the embedded processor via an internal bus;

wherein the array processor comprises:

a first multiply/accumulator (MAC) unit coupled to a first local memory, the first local memory comprising a first plurality of operands;

a second MAC unit coupled to a second local memory, the second local memory comprising a second plurality of operands; and

a first shared operand unit coupled to the first MAC unit and the second MAC unit for providing a first shared operand to the first MAC unit for computing a first result in association with the first plurality of operands and to the second MAC unit for computing a second result in association with the second plurality of operands; and

wherein the first result and the second result are computed independently of each other; and

wherein the array processor further comprises:

a second shared operand unit coupled to a third MAC unit and a fourth MAC unit for providing a second shared operand to the third MAC unit and the fourth MAC unit.

Received from < 6503262422 > at 4/23/02 12:04:27 AM [Eastern Daylight Time]

12. (Amended) The integrated circuit according to claim 10 wherein a first instruction stream and a first data stream is maintained for said array processor, and a second instruction stream and a second data stream is maintained for said embedded processor.

16. (Amended) The integrated circuit according to claim 10 further comprising:

a global external bus unit for providing an interface to said integrated circuit, said global external bus unit coupled to said embedded microprocessor by a system bus and by a separate dedicated bus.

Received from < 6503262422 > at 4/23/02 12:04:27 AM [Eastern Daylight Time]